Design and Comparative Analysis of 7nm SRAM Cells using Double Gate FinFET Technology for Low- Power Memory Applications

B. Saritha
Department of ECE
Vaagdevi College of Engineering
Telangana, India.
balabadrasaritha@gmail.com

Dr.B. Satheesh
Assistant professor
Vaagdevi College of Engineering
Telangana, India
Satheesh_b@vaagdevi.edu.in

Abstract: ***As semiconductor technology scales into the deep nanometer regime, Static Random Access Memory (SRAM) cells encounter increasing challenges such as leakage current, read instability, and degraded performance caused by short-channel effects. This paper presents a 7nm Double-Gate (DG) FinFET-based proposed 8T SRAM cell designed to achieve low power consumption and high-speed operation. The proposed architecture improves the conventional 8T SRAM by incorporating an optimized decoupled differential read path and enhanced transistor sizing while preserving the standard eight-transistor configuration. The differential read architecture employs complementary read bit lines (RBL and RBLB), enabling non-destructive read operations with improved sensing accuracy and enhanced Read Static Noise Margin (RSNM). Furthermore, the use of DG FinFET technology provides superior gate control, reduced leakage current, and improved switching characteristics compared with conventional planar CMOS devices.The proposed SRAM cell was designed and simulated using 7nm FinFET technology in the Cadence Virtuoso environment. Simulation results demonstrate significant improvements over the conventional 8T SRAM. The proposed design reduces the write power from 3.340 µW to 1.756 µW (approximately 47.4% reduction) and the read power from 21.94 µW to 4.80 µW (approximately 78.1% reduction). In addition, the write delay is reduced from 2.44 ns to 8.25 ps, while the read delay is slightly improved from 12.77 fs to 12.71 fs. These improvements are achieved through optimized differential read circuitry and transistor sizing without increasing the transistor count. Therefore, the proposed DG FinFET-based 8T SRAM cell offers an efficient combination of low power consumption, high read stability, and high-speed operation, making it well suited for cache memories, embedded processors, Internet of Things (IoT) devices, and other advanced VLSI applications.***

Keywords: ***7nm FinFET, Double-Gate FinFET, 8T SRAM, Differential Read Architecture, Low Power, High Speed, Read Stability, Leakage Reduction, Cadence Virtuoso, VLSI.***

I. INTRODUCTION

Static Random Access Memory (SRAM) is a crucial memory component that is employed in microprocessors, cache memories, embedded systems, portable devices, IoT nodes, and system-on-chip architectures.Modern SoCs have been developed to address the demands of various applications and settings. These vary from the relatively secure and intricate automotive systems, to more limited handheld gadgets, and extend to independent network-connected nodes. Each has distinct security needs concerning the storage, processing, along with transmission of confidential data. Consequently, the safety of these computer networks has emerged as a persistent issue for both academia and the commercial sector. [1], [2].

SRAM is used often in computation and its energy consumption and delay directly impact the overall energy efficiency and speed of a digital system. In the modern VLSI circuits, memory arrays consume a significant amount of chip area and hence low power and high speed SRAM design is an important requirement.

The 6T SRAM cell is widely used due to its simple structure, small area and ease of implementation of the memory array. As technology shrinks to deep nanometer dimensions, however, the 6T cell has a number of issues, such as increased leakage current, reduced read stability, poor write ability, process variation, and reduced Static Noise Margin (SNM). The 6T SRAM cell is a cell that uses the same access transistors for both reading and writing. Consequently, the ability to read and write the data is strongly dependent on the size of the transistors. Strengthening the access transistor makes it easier to write data, but can cause data to be disturbed when reading it, and strengthening the pull-down transistor makes it easier to read data, but can make it harder to write data .

However, planar CMOS technology has its limitations and FinFET devices have been found to be appropriate for nanoscale SRAM design. The advantages of FinFETs over traditional MOSFETs are improved gate control, reduced short-channel effects, lower leakage current and scalability. Therefore, the SRAM cells based on FinFETs are extensively explored for low power and high-performance memory applications. The read stability, write ability and SNM are important design parameters for the sub-10 nm domain studies of FinFET based SRAM [1,2]. FinFET SRAM macros have also been shown for advanced nodes like 14 nm and 3 nm for low voltage memory operation [3, 4, 11]. The structural differences between the planar MOSFETs and the FinFET devices as shown in Fig. 1.

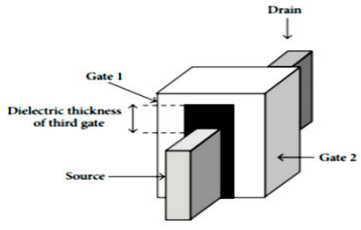

Figure 1.The structural design of DG FinFET device

The DG FinFET is called a single-gate design because its Fin) is much larger than its height (HFin), and the gate oxides on the sidewalls are significantly thicker than those on top.FinFET based SRAM is strategically designed to replace CMOS based SRAM cells[7]. The objective is to achieve lower power consumption,minimize data noise, and optimize data retention voltage[7].The average power dissipation, denoted as P_{avg} is represented in (3).

$$P_{avg} = \frac{1}{T}\int V * I(t)\, dt$$

Where, f (1/T) is frequency, I denotes the current and V the supply voltage.

To overcome the drawbacks of the conventional 6T SRAM, several SRAM topologies like 7T, 8T, 9T and 10T cells have been proposed. The 8T SRAM cell is one of them that offers an attractive feature of having a separate read path, thereby minimizing read disturbance and enhancing data stability. Additional transistors, however, will require additional area and may add power or delay overhead. So, the design of SRAM should be a compromise between power consumption, delay, stability and area.

This work has made the following key contributions:

- Design and comparison 8T SRAM cells with 7nm FinFET technology.
- Instead of one read bit line (RBL),the proposed design has RBL , RBLB (Read Bit Line Bar) .This forms a Differential Read Scheme.for SRAM power reduction.
- Proposed 8T SRAM cell is a balanced structure for low power and high-speed memory application.

II. CO-RELATED WORK

A lot of attention has been paid to SRAM configurations at advanced nanoscale technology nodes because they are prone to soft errors caused by strong particles in harsh radiation environments.The SRAM-dependent memory arry radiation environments. The SRAM-dependent memory array is the processor's biggest memory component. This leads to increased leakage and fluctuating power usage throughout the system. Thus, it optimizes processing power, size, and speed. Chip efficiency depends on circuit size, power consumption, and speed. Thus, cache memory must be small, power-efficient, fast, and error-resistant to achieve a processor with a higher processing speed.These investigations suggest modified SRAM cells [7].

6T SRAM memory cells with positive feedback can't handle SEUs [8]. This is because changing the potential in one node flips over the potentials in all the other nodes.The 8T SRAM cell proposed here has a number of design and device-level innovations that make it stand out in comparison to other 8T, 7T, and 6 T designs reported before. Its main innovation is that the read transistors are connected differently,Instead of sensing only one storage node,Both Q &QB participate in the read operation.This produces a stronger voltage difference.Rather than single-ended sensing,the proposed SRAM uses Differential Read Technique where RBL &RBLB are compared by a differential sense amplifier.

There have been a number of studies on SRAM design techniques to reduce power consumption, improve read stability and enhance write performance in scaled technologies. Recent SRAM research demonstrates that leakage power, reading disturbance, writing issues, along with standby power remain key challenges in scaled memories. Surekha et al. [9] developed a 7T SRAM cell with two memory nodes. To modify the 6T SRAM circuit, they connected an NMOS transistor to the voltage source of the two pull-up PMOS transistors. Another NMOS transistor's gate terminal is connected to source voltages and word lines. The design uses less power and improves SNM compared to 6T SRAM cells in hold, reading, and writing modes. Vasudeva Reddy et al. [10] introduced 256 Schmitt trigger-dependent 8T cells, but 256-bit unit pull-down devices make up an 8T bit cell. Their designs focus more on energy utilization, latency, and noise margin than radiation resistance; however, power dissipation has decreased. Nagma Sahi et al. [11] designed a SRAM unit with four memory terminals, four PMOS pull-ups, six NMOS pull-downs, and cascade transistors. They have shown that, because of the stacked NMOS transistors, the design takes longer to switch off during reading operations, increasing read access. Unfortunately, it is surrounded by NMOS and PMOS, increasing the number of node pairs.

E. Mani et al. [11] introduced an advanced 8 T SRAM unit utilizing Fin FET technology. This unit includes distinct pathways for reading and writing activities, facilitating independent engagement. The implementation of single-ended memory designs can significantly decrease power consumption. The vertical arrangement of transistors, along with the absence of bit-line leakage, significantly diminishes power leakage.

Rawat et al. [1] suggested for the SRI approach, which is essential for enhancing stability, resulting in the proposed 8T SRAM cell outperforming its 6T SRAM counterpart. The enhanced efficiency achieved by the proposed 8T SRAM cell necessitates the addition of four additional transistors. Simulations utilizing 90 nm technology have been conducted to evaluate the effectiveness of the Restoration Inverter method in decreasing power consumption and enhancing stability in SRAM cells.

From the literature, it is evident that 6T SRAM offers a small area, but has read/write compromises at scaled nodes. With FinFET technology, leakage and scalability are enhanced, and with 8T SRAM, read stability is enhanced by having a separate read path Hence, the present work suggests an optimized 8T SRAM in7nm FinFET technology to minimize the read power consumption with high-speed operation.

III. EXISTING SRAM CONVENTIONAL CELLS

3.1. Existing 8T SRAM

Two CMOS cross-coupled inverters are used in the architecture of the 1-bit 6T SRAM to function as a latch. The data to be preserved is latching onto these two inverters. Latch perform different operations, i.e. Read, Write & Hold. This latch is operated by internal pulse provided to it. Its two access transistors are used to access Bit Line, Bit Line Bar(both BL & BLB function according to WL).[6] The fundamental design of a 8Tcell is seen in Figure 2.

The transistors M0, M1, M2 and M3 are the main cross-coupled inverter pair for data storage in the 8T SRAM cell as depicted in Figure 2. Here, M0 and M2 are PMOS pull-up transistors, while M1 and M3 are NMOS pull-down transistors. The write access transistors M5 and M4 are connected to BLB and BL and are controlled by the write word line WWL [5]. Apart from this, transistors M6 and M7 are connected to the read bit line RBL and are controlled by the read word line RWL.

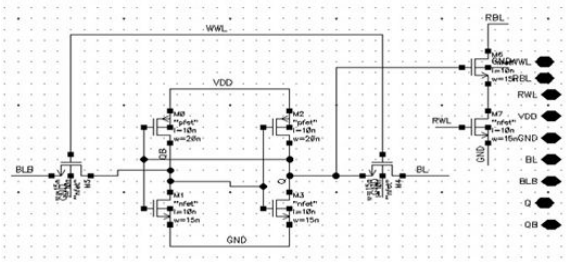

Figure 2: Circuit of existing 8T SRAM Cell

In hold operation, WWL and RWL are low, which means that the write access path and read path are both disabled. The data is stored at Q and QB by the cross coupled inverter pair. When writing, WWL is turned on, and the data is written via M5 and M4 from BLB and BL to the storage nodes. In the read operation,show in figure 3, the write access transistors are kept OFF and only the separate read path made up of M6 and M7 is used. If the stored data allows the read discharge path, then the read transistors discharge the data, otherwise it stays high. Since the internal storage nodes are not directly disturbed during reading, the 8T SRAM cell provides better read stability than 6T and 7T SRAM cells [19]. The drawback of the 8T SRAM cell is that it requires two extra transistors, an extra read word line, and an extra read bit line, which leads to higher area, routing complexity, and peripheral circuit requirements.

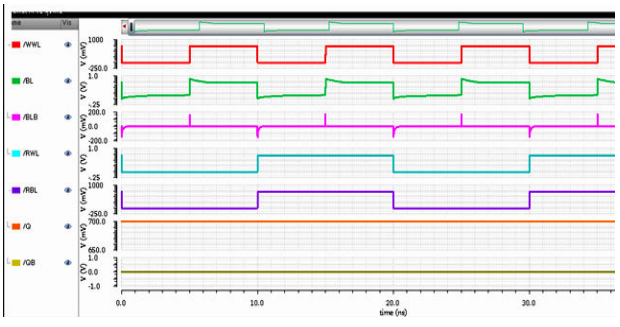

Figure 3 : Read operation of 8T SRAM

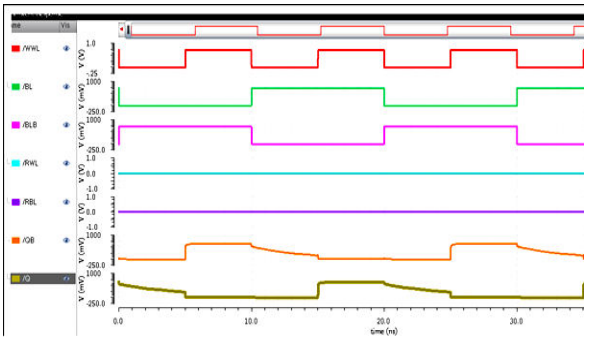

Figure 4 : Write operation of 8T SRAM

IV. THE PROPOSED 8T SRAM CELL

The proposed 8T SRAM cell is show in figure 5, composed of a conventional 6T cross-coupled inverter pair for data storage, along with an additional 2T read port that enables a decoupled read operation.

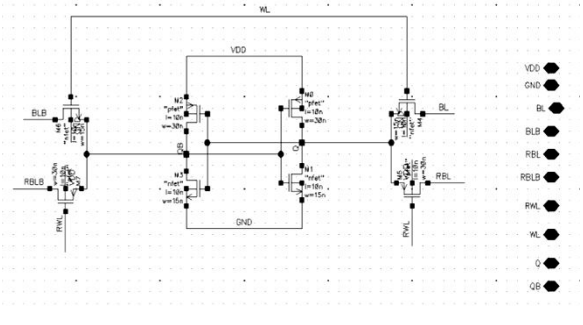

Figure 5: Schematic of proposed 8T SRAM

During the hold state, the word line (WL) remains low, thereby isolating the storage nodes from the bit-lines, while the cross-coupled inverters maintain the stored data. In the write operation, WL is asserted high, allowing the bit-line pair (BL and BLB) to force the desired logic value into the internal storage nodes (Q and QB).

4.1. Operation of Proposed 8T SRAM:

Hold Operation

During the hold mode, both the Word Line (WL) and Read Word Line (RWL) are kept LOW, turning OFF the write and read access transistors. The cross-coupled inverters retain the stored data without any interaction with the bit lines. As a result, the cell maintains its stored value with very low leakage power and high data stability.

Write Operation

During the write operation, the Read Word Line (RWL) remains LOW while the Word Line (WL) is asserted HIGH. The complementary data applied to the bit lines (BL and BLB) are transferred to the internal storage nodes (Q and QB) through the write access transistors. The cross-coupled inverters reinforce the new logic state, and the data is stored once WL returns LOW.

Read Operation

Before the read operation, both Read Bit Lines (RBL and RBLB) are precharged to the supply voltage. The Word Line (WL) remains LOW to isolate the storage nodes from the write bit lines, while the Read Word Line (RWL) is asserted HIGH. Depending on the stored data, one of the read bit lines discharges while the other remains at the precharged level. A differential sense amplifier detects the voltage difference between RBL and RBLB to determine the stored logic value. Since the storage nodes are isolated from the read path, the proposed SRAM cell achieves higher Read Static Noise Margin (RSNM), faster read access, improved noise immunity, and lower read power compared to the conventional 8T SRAM cell.

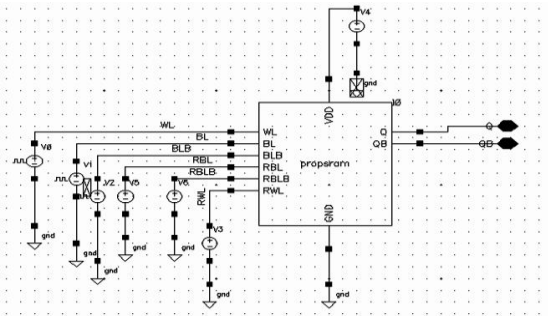

Figure 6. Logic diagram of proposed 8T SRAM cell

Unlike conventional 6T SRAM cells, the proposed design ensures that the internal storage nodes are electrically isolated from the read bit-line (RBL), which remains floating during the read phase. Depending on the stored data, the read path either allows or restricts current flow, resulting in a detectable voltage change on RBL without disturbing the stored information. This decoupled read mechanism effectively eliminates the read disturb issue, enhances the read static noise margin, and enables reliable operation at lower supply voltages. Furthermore, the behavior of the read bit-line can be exploited for logic-in-memory applications, making the proposed architecture suitable for energy-efficient and high-performance computing systems.The proposed 8T SRAM that introduces a differential read technique using RBL and RBLB. By reading both Q and QB simultaneously and using a differential sense amplifier, it achieves faster read speed, higher read stability, improved noise immunity, and potentially lower read power.

V. SIMULATION RESULTS

The designed and simulated proposed 8T SRAM cells were designed and simulated in Cadence Virtuoso circuit design environment with 7nm FinFET technology. The first implementation of the existing 8T SRAM cells was done using FinFET devices in this work. Basic performance values of these conventional SRAM cells were obtained and Lastly, the optimized proposed 8T SRAM was simulated and compared to the existing SRAM cells. This work also presents the implementation

of the 8T SRAM cells in Cadence Virtuoso and FinFET devices in 7 nm technology.

The simulation was performed at the circuit level, the schematic of the SRAM was designed and appropriate write, read and standby signals were applied. The conventional 8T SRAM cells were developed with no add additional transistors to enhance control and read stability. The proposed 8T SRAM cell exhibits significant improvements over conventional 6T and previously reported modified SRAM architectures, primarily due to its fully decoupled read mechanism. In a standard 6T SRAM cell, both read and write operations are performed through the same access transistors controlled by a single word line, which directly connects the internal storage nodes to the bitlines. This shared path results in a read disturb issue, where the stored data can be inadvertently altered during read operations, particularly under low supply voltage conditions. The existing modified SRAM structures attempt to mitigate this limitation by introducing additional transistors or control signals; however, they still retain partial interaction between the read path and the storage nodes, thereby offering only moderate improvement in stability and noise margin.

In contrast, the proposed 8T SRAM architecture introduces a dedicated read port consisting of separate read word lines (RWL) and read bit-lines (RBL/RBLB), completely isolating the storage nodes from the read path. The core storage element remains a cross-coupled inverter pair, ensuring robust data retention, while the write operation is performed conventionally through the bit-lines BL and BLB under the control of the write word line (WL). During the read operation, both BL and BLB are precharged, and the read bit-line is left floating. When the read word line is activated, the voltage on the read bit-line changes conditionally based on the stored data, without directly disturbing the internal storage nodes. This decoupled operation effectively eliminates read disturb, enhances the read static noise margin, and enables reliable operation at reduced supply voltages.The write and read operations of the proposed SRAM cell are demonstrated in Figure 9 and 10 respectively.

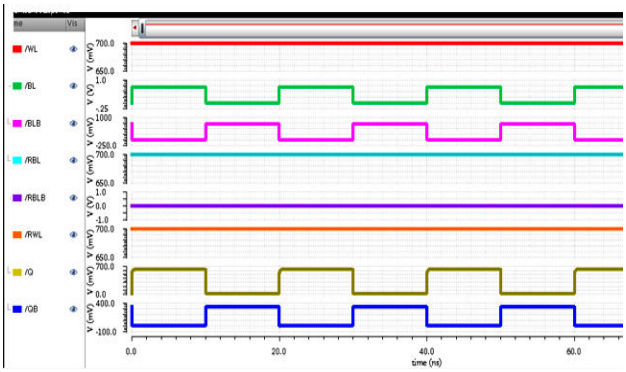

Figure 9: Write Operation of proposed 8T SRAM

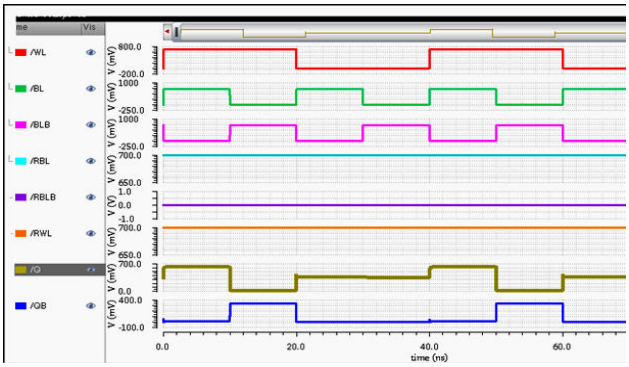

Figure 10: Read Operation of proposed 8T SRAM

Table 1. The final comparison of the performances of SRAM cells

SRAM Type	Write Power (µW)	Read Power (µW)	Write Delay	Read Delay
8T SRAM	3.340	21.94	2.44 ns	12.77 fs
Proposed 8T SRAM	**1.756**	**4.80**	**8.25 ps**	**12.71 fs**

Table 1. shows that power and speed performance compared with 8T SRAM cells and the Proposed 8T SRAM achieves a breakthrough in power consumption, reducing Write Power by ~47.4% and Read Power by ~78.1% compared to the standard 8T model.Proposed 8T SRAM breaks the traditional trade-off between power and performance. It delivers the lowest read power and fastest read speed . while successfully fixing the extreme write-delay issues typically found in standard 8T architectures.

The proposed 8T SRAM cell employs a decoupled differential read architecture using two dedicated read bit lines (RBL and RBLB). During the read operation, the

write access transistors remain OFF while the read word line activates the separate read transistors, ensuring that the internal storage nodes are isolated from the bit lines. This eliminates read disturbance and significantly enhances the Read Static Noise Margin (RSNM). Furthermore, the differential sensing mechanism provides faster read access, improved noise immunity, reduced read delay, and reliable low-voltage operation compared to the conventional single-ended 8T SRAM architecture.

VI. CONCLUSION

The paper gives a detailed analysis of the performance, power efficiency and stability of 8T SRAM cells using FinFET technology at the 7nm node. It shows a few advantages of FinFET in regard to leakage current suppression, superior switching characteristics, and robustness improved in SRAM designs. The 8T configuration is the standard design, compact, and energy-efficient.In this paper, a high-performance, low-power 8T SRAM architecture was evaluated and compared against standard 8T SRAM designs. Simulation data confirms that the proposed architecture successfully breaks the conventional power-delay product (PDP) trade-off. By lowering write power by 47.4% and read power by 78.1%, alongside reducing write delay from 2.44ns to 8.25ps, the proposed cell establishes a superior design point for energy-constrained, high-throughput memory arrays suitable for wearable systems, mobile processors, and edge computing nodes.

The proposed design reduces dynamic power consumption by limiting unnecessary switching activity on the main bit-lines during read operations and confines the sensing activity to the read bit-line. The use of a separate read path also improves read speed due to direct sensing and reduced capacitive loading. Additionally, the dynamic behavior of the read bit-line makes the architecture suitable for logic-in-memory and compute-in-memory applications, which are not feasible with conventional SRAM designs. The trade-off is justified by the substantial gains in stability, power efficiency, and scalability, making it a promising candidate for advanced low-power memory and computing systems.according to simulation data, especially in very high-speed, low-power applications. In this way, one demonstrates a possibility to optimize the designs of SRAM memory cells for future semiconductor technologies according to increasing demand in the field of high-density, energy-efficient solutions. Future work can be found in scaling challenges, temperature variations, and integration with advanced logic circuits for further extension of applicability of these designs in the cutting-edge computing systems.

REFERENCES

[1] “Ultra Low Power SRAM Cell for High Speed Application using 90nm CMOS Technology” proposed by Hansraj,Ajay Rana , 2021.

[2] T. Wada, S. Rajan, and S. Przybylski, “An analytical access time model for on-chip cache memories,” IEEE J. Solid State Circuits, vol. 27, no. 8, pp. 1147–1156, Aug. 2022

[3] “Static Noise Margin Analysis of SRAM Cell For High Speed Application”, Debasis Mukherjee, Hemanta Kr.Mondal 2021 IJCSI.

[4] “Design and analysis of 6T SRAM in 45 nm Technology”, V. Panduranga Vemula, S. Priyanka, A. Sairam , IJERT,2022.

[5]. V. Panduranga and C. Prathyusha, “Design and Implementation of 8T SRAM at 18nm FINFET Technology in Cadence Virtuoso,” International Journal of Engineering Research & Technology, vol. 11, no. 5, pp. 448–452, 2022.

[6]. Y. Ma, L. Zhang, and J. Liu, “A New 6T SRAM Memory Cell Based on FINFET Process,” 2020 5th International Conference on Integrated Circuits and Microsystems, ICICM 2020, pp. 251–254, 2020.

[7]. Deepak Garg1, Rupali Singh1, Devendra Kumar Sharma2 Analysis of FinFET based SRAM cells with improved performance parameters Indonesian Journal of Electrical Engineering and Computer ScienceVol. 37, No. 3, March 2025, pp.1464~1475ISSN:2502-4752,

DOI:10.11591/ijeecs.v37.i3.pp1464-1475 ·

[8]. T. S. Kumar and S. L. Tripathi, “Comprehensive Analysis of 7T SRAM Cell Architectures with 18nm FinFET for Low Power Bio-Medical Applications,” Silicon, vol. 14, no. 10, pp. 5213–5224, 2022.

[9]. T. V. Lakshmi and M. Kamaraju, "A Review on SRAM Memory Design Using FinFET Technology," International Journal of System Dynamics Applications, vol. 11, no. 6, pp. 1–21, 2022.

[10]. Dhori K. J., Chawla H., Kumar A., Pandey P., Kumar P., Ciampolini L., Cacho F., Croain D., "High-yield design of high-density SRAM for low-voltage and low-leakage operations," IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT), pp. 1-6, 2018, DOI: 10.1109/DFT.2017.8244429.

[11]. P. Singh and S. K. Vishvakarma, "Ultra-Low Power High Stability 8T SRAM for Application in Object Tracking System," IEEE Access, vol. 6, pp. 2279– 2290, 2018.

[12]. S. R. Mansore, "A Single-Ended Read Decoupled 9T SRAM Cell for Low Power Applications," in IEEE International Symposium on Nanoelectronic and Information Systems, 2017, pp. 220–223.

[13]. C. Huang, K. Wu, C. Wu, and L. Chiou, "Ultra-Low Standby Power SRAM with Adaptive Data-Retention-Voltage-Regulating Scheme," in EEE International Symposium on Circuits and Systems, 2018, pp. 0–3.

[14].D. Garg, R. Singh, and D. K. Sharma, "Analysis of FinFET based SRAM cells with improved performance parameters," Indonesian Journal of Electrical Engineering and Computer Science, vol. 37, no. 3, pp. 1464–1475, Mar. 2025.

[15]. S. S. Ensan, A. Ghaffari, and R. Doost-Mojdehi, "A low-power single-ended SRAM in FinFET technology," AEU – Int. J. Electronics and Communications, vol. 113, p. 152970, 2019.

[16]M. A. Turi and J. G. Delgado-Frias, "Effective low-leakage 6T and 8T FinFET SRAMs using reverse-biased FinFETs and power gating," IEEE Trans. Circuits Syst. II, vol. 67, no. 4, pp. 765–769, 2020.

[17]. T. V. Lakshmi and M. Kamaraju, "A review on SRAM memory design using FinFET technology," Int. J. System Dynamics Applications, vol. 11, no. 6, pp. 1–21, 2022.

[18]. F. Moradi et al., "Asymmetrically doped FinFETs for low-power robust SRAMs," IEEE Trans. Electron Devices, vol. 58, no. 12, pp. 4241–4249, Dec. 2011.

[19].S. Birla, N. K. Shukla, and N. Singh, "Performance analysis of 8T FinFET SRAM bit-cell for low-power applications," Proc. ICCCS, pp. 1–4, Oct. 2020.

[20].J. Jiang et al., "Quadruple cross-coupled latch-based 10T and 12T SRAM bit-cell designs for highly reliable terrestrial applications," IEEE Trans. Circuits Syst. I, vol. 66, no. 3, pp. 967–977, Mar. 2019.

[21].S. Ahmad, M. K. Gupta, and M. Hasan, "Single-ended Schmitt-trigger-based robust low-power SRAM cell," IEEE Trans. VLSI Systems, vol. 24, no. 8, pp. 2634–2642, Aug. 2016.

[22].X. Xue et al., "Design and performance analysis of 32×32 memory array SRAM for low-power applications," Electronics, vol. 12, no. 4, p. 834, Feb. 2023.

[23].G. Ravikishore and N. M. Nandhitha, "6T-SRAM design to optimize delay using FinFET technology," Proc. ICICV, pp. 540–544, Feb. 2021.

[24].R. R. Vallabhuni et al., "Comparative validation of SRAM cells designed using 18 nm FinFET for memory storing applications," SSRN Journal, 2020.

[25]H. Amrouch et al., "Impact of variability on processor performance in negative capacitance FinFET technology," IEEE Trans. Circuits Syst. I, vol. 67, no. 9, pp. 3127–3137, Sep. 2020.

[26].M. V. N. Rao et al., "Design and development of efficient SRAM cell based on FinFET for low power memory applications," Journal of Electrical and Computer Engineering, 2023